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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,841	06/08/2000	Warren M. Farnworth	3923US (99-0033)	1415

7590 05/22/2002

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EXAMINER
LEE, GRANVILL D

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/589,841	FARNWORTH ET AL.	
	Examiner	Art Unit	
	Granvill D Lee, Jr	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) *38-51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37 and 52-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/8/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *23 January 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 9 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

The newly submitted specification, although entered, was not accessible to be review at the time of the initial office action. The office appreciates making it aware, as further correspondences should reflect the updated specification and examination of claims 1-37 and 52-56.

Response to Applicant's Argument

After review of applicant's amendments and comments, the examiner finds such arguments unpersuasive. Applicant's comments as to Fjelsted, Farnworth and Hull are well taken, however in further review of the prior art, the examiner has found that Grigg et al., Spence et al., Fjelsted and DiStefano et al. read upon applicant's claimed invention. As these are a new grounds for rejection, but the following rejections are not to be considered final.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Applicant has provided evidence in this file showing that the invention was owned by, or subject to an obligation of assignment to, the same entity as

6,337,122 at the time this invention was made. Accordingly, 6,337,122 is disqualified as prior art through 35 U.S.C. 102(e), (f) or (g) in any rejection under 35 U.S.C. 103(a) in this application. However, this applied art additionally qualifies as prior art under another subsection of 35 U.S.C. 102 and accordingly is not disqualified as prior art under 35 U.S.C. 103(a).

Applicant may overcome the applied art either by a showing under 37 CFR 1.132 that the invention disclosed therein was derived from the inventor of this application, and is therefore, not the invention "by another", or by antedating the applied art under 37 CFR 1.131.

Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grigg et al. (US Pat. 6,337,122) in view of Fjelstad (US Pat. 6,284,563).

In view of claims 1, 8 and 12-13, Grigg et al. teaches that an intricate stereolithographic technique that can be used to cover or mark a plurality of devices (Fig. 8 #30), by forming at least one layer (with subsequent mutual layers adhering to each other (Col. 4 lines 15-20) (clm. 8)) made of a liquid or unconsolidated material (Fig. 9 #86) over a portion of the device (Col. 8 lines 40-54) and then selectively altering the state of that first layer from an unconsolidated state to a consolidated state (Col. 9 line –Col. 10 line 17) at desired locations. However, Grigg et al. does not describe the technique in terms applying it to at least one bond or active surface pad as a protective layer. But, Fjelstad describes a process where a dielectric protective compliant layer is placed over a semiconductor chip (Col. 3 lines 20-25), having at least

one bond pad (Fig. 2 #110). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the teachings of Grigg et al. with those of Fjelstad with the intention of having better access results, since the purpose of Fjelstad was to use a protective layer (Col. 3 lines 18-40) over devices with a multitude of apertures where the contacts within them could be accessed (Col. 4 lines 21-30).

In view of claim 2, Grigg et al. shows that the first layer is a liquid layer applied to the surface of a device (Col. 10 lines 40-65).

In view of claims 3 and 6, Grigg et al. explain that a portion of an unconsolidated liquid layer, where additional layers can be of similar thicknesses (Col. 10 lines 15-20), and partially cured to a semisolid state (Col. 9 lines 15-20).

In view of claims 4, 5 and 23, Grigg et al. employs a UV laser under computer control to direct its energy to cure the layer (Col. 9 lines 7-23).

In view of claim 7, Grigg et al. illustrates a wafer (Fig. 8 #72) with a plurality of semiconductor devices (#30) or dice thereon (Col. 7 lines 20-30).

In view of claims 9 and 14, Grigg et al. shows that removal of one or more layers is possible (Fig. 1 #19).

In view of claims 10 and 15, the Grigg et al. process shows that the partially cured layers can be fully cured (Col.9 lines 7-23) or post-cured (Col. 14 lines 38-40).

In view of claims 11 and 22, Fjelstad depicts the bond pads (Fig. 2 #110) or active surface, protected by the process taught by Grigg et al. indicated above in claim 1.

In view of claims 16-19, Grigg et al. discloses a process (Col. 7 lines 24-30) before or after singulation (Fig. 8).

In view of claims 20 and 21, Grigg et al. selectively alters layers by overlaying the device or wafer with a platform layers, then follow with liquid layers (Col. 10 lines 17-65).

Claims 24-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grigg et al. (US Pat. 6,337,122) in view of Fjelstad (US Pat. 6,284,563) in further view of Kaldenberg (US Pat. 5,897,338).

Grigg et al. teaches, in view of claims 24, 29 and 33, that an intricate stereolithographic technique that can be used to cover or mark a plurality of devices, by forming at least one layer (with subsequent mutual layers adhering to each other) is made of a liquid or unconsolidated material over a portion of the device and then selectively altering the state of that first layer from an unconsolidated state to a consolidated state at desired locations. Fjelstad describes a process where a dielectric protective compliant layer is placed over a semiconductor chip, having at least one bond pad and other active areas for device development. However, neither Grigg et al. or Fjelstad utilize a process where a lead frame portion of a package is explicitly covered. Yet, Kaldenberg

reveals a process that encapsulates a semiconductor chip with a lead frame (Col. 1 lines 5-10). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the inventions of Grigg et al. and Fjelstad, with the teachings of Kaldenberg with the desire of bring out better encapsulating results, because the process suggested by Kaldenberg will encapsulate the entire semiconductor circuit completely with the flexibility to encompass other devices (Col. 1 lines 5-35) or portions thereof.

In view of claim 25, Grigg et al. employs a UV laser under computer control to direct its energy to cure the layer (Col. 9 lines 7-23).

In view of claims 26-28, Grigg et al. explains how the camera system (Fig. 9 #140) can be activated to locate the position and orientation of each device or substrate (Col. 12 lines 37-50).

In view of claim 30, Grigg et al. shows that removal of one or more layers is possible (Fig. 1 #19).

In view of claims 31 and 32, the Grigg et al. process shows that the partially cured layers can be fully cured (Col.9 lines 7-23) or post-cured (Col. 14 lines 38-40).

In view of claims 34 and 35, Grigg et al. explains how the camera system (Fig. 9 #140) can be activated to locate the position and orientation of each device or substrate (Col. 12 lines 37-50), and further stores that data in a memory storage area of the assembly (Col. 12 lines 37-67).

In view of claims 36 and 37, Grigg et al. depicts a platform system that horizontally secures the wafer (Fig. 9 #90) and lowers the wafer of device into a bath for further stereolithographic processing (Col. 10 lines 40-60).

Claims 52-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grigg et al. (US Pat. 6,337,122) in view of Fjelstad (US Pat. 6,284,563) in further view of DiStefano et al. (US Pat. 6,045,655).

Grigg et al. teaches, in view of these claims, that an intricate stereolithographic technique that can be used to cover or mark a plurality of devices, by forming at least one layer is made of a liquid or unconsolidated material over a portion of the device and then selectively altering the state of that first layer from an unconsolidated state to a consolidated state at desired locations. Fjelstad describes a process where a dielectric protective compliant layer is placed over a semiconductor chip, having at least one bond pad and other active areas for device development. But, both inventors fails to describe an alignment means between components. However, DiStefano et al. in the process of providing an adhesive or compliant layer (Fig. 17 #430) to semiconductor chips mounted on a package, DiStefano et al. aligns some components to other components and maintains the alignment. (Col. 16 lines 50-60). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the inventions of Grigg et al. and Fjelstad, with the teachings of DiStefano et al. with the objective of revealing

better alignment results, since it is easier to align components already aligned, rather than align each component from the start or disturbing the alignment already achieved (Col. 4 lines 6-31).

Contact Information

Any inquiry concerning this communication or earlier communications for the examiner should be directed to Granvill Lee whose telephone number is (703) 306-5865. The examiner can be normally reached on Monday thru Thursday from 7:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are not successful, the examiner's supervisor, Matthew Smith can be reached on (703) 308-1323. The fax phone number for this group is (703) 308-7722.

Any inquiry of a general nature relating to status or otherwise should be directed to the receptionist whose telephone number is 703-308-1782.

Examiner
Granvill Lee
Art Unit 2825

Gl
5/7/02

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